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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/758,675	01/11/2001	Klaus Gloeckler	10191/1639	9544

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EXAMINER	
TORRES, JOSEPH D	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 07/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/758,675	GLOECKLER ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-10 and 12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-10 and 12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1, 3-10 and 12 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1, 3-10 and 12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1 and 10 recite, "the boundary scan test procedure may occur without external access to the JTAG interface". A boundary scan test procedure is just a procedure or abstract method and is not external or internal to any circuitry, hence it is not clear what is meant by "the boundary scan test procedure may occur without external access to the JTAG interface".

In addition, "may occur" is indefinite since the term "may" expresses an indefinite probability of occurrence.

Claims 1, 3-10 and 12 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between

the elements. See MPEP § 2172.01. Claims 1 and 10 recite, "the boundary scan test procedure may occur without external access to the JTAG interface". The omitted elements are: specific hardware elements used in a boundary scan test procedure in order to gauge what is meant by "the boundary scan test procedure may occur without external access to the JTAG interface" since what is probably meant is that internal scan circuitry does not rely on external access to the JTAG interface during a particular microprocessor-initiated boundary scan test procedure.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1, 3-8, 10 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Whetsel; Lee D. (US 6408413 B1) in view of Hellebrand et al.

(Hellebrand, S.; Wunderlich, H.-J.; Hertwig, A.; **Mixed-mode BIST using embedded processors,** Proceedings International Test Conference, 20-25 Oct. 1996 Page(s):195 – 204, hereafter referred to as Hellebrand).

35 U.S.C. 103(a) rejection of claim 1.

Whetsel teaches a method for activating a IC core circuitry, within a framework of a boundary scan test procedure as set forth in IEEE standard 1149 using a JTAG interface of the microprocessor (the Abstract and Figure 2 of Whetsel teaches a device for activating IEEE 1149.1 compliant test access ports for an IC comprising multiple IEEE 1149.1 compliant test access ports for testing core circuitry in the IC as shown in Figure 18 of Whetsel; Col. 17, lines 7-36 in Whetsel teach an application and embodiment whereby the IC is a microprocessor; Note: an IEEE 1149.1 compliant tests access port is a JTAG interface, hence Whetsel teaches a method for activating a microprocessor for Boundary Scan testing, within a framework of a boundary scan test procedure as set forth in IEEE standard 1149 using at least one IEEE 1149.1 compliant test access port of the microprocessor, i.e., at least one JTAG interface), comprising the step of: activating the JTAG interface of IC core circuitry with a test routine that is executable on the IC core circuitry (the Abstract and Figure 2 of Whetsel teaches that TAP linking module 21 is used for activating at least one IC IEEE 1149.1 compliant test access ports, i.e., at least one JTAG interface; col.4, lines 25-28 in Whetsel teach that during testing the TLM is selected as the data register's scan path between the IC's TDI and TDO scan path used for providing the IC with test routine data; col.4, lines 40-42 in

Whetsel teach that test routine data provided to the TLM on the TDI input is used to select one of the 4 enable signals EN1-4 for activating at least one of the IC IEEE 1149.1 compliant test access ports corresponding to the enable signal); and transmitting a test data stream provided by the test routine to the JTAG interface from IC core circuitry (each of the TDO1-TDO4 test data outputs in Figure 2 of Whetsel provides a means for transmitting a test data output stream in response to test routine data inputted at TDI 26 to the JTAG interface from IC core circuitry); wherein I/O ports of the IC core circuitry are connected to pins of the JTAG interface (Note: each of the I/O ports, TDI, TDO1-TDO4 of the IC core circuitry are connected to TDI pin 26 and TDO pin 27 hence TDI pin 26 and TDO pin 27 are pins for each of the TAP1-TAP4 JTAG interfaces, that is, I/O ports, TDI, TDO1-TDO4, of the IC core circuitry are connected to TDI pin 26 and TDO pin 27 pins of the JTAG interface), and a data-in pin of the JTAG interface is activated using the test routine via the I/O ports (TDI pin 26 is the data-in pin for each of the TAP1-TAP4 JTAG interfaces, hence when any of the TAP1-TAP4 JTAG interfaces are activated, the TDI data-in pin 26 for the activated TAP1-TAP4 JTAG interfaces is also activated to provide test routine data to the activated TAP1-TAP4 JTAG interfaces and is activated using the test routine data by providing the test routine data to the TLM).

However Whetsel does not explicitly teach that the IC taught in the Whetsel patent is a microprocessor arranged as a part of a microcontroller.

Webopedia (http://www.webopedia.com/TERM/m/microcontroller.html) defines a microcontroller as a highly integrated IC chip that contains all the components

comprising a controller, typically, including a CPU, RAM, some form of ROM, I/O ports, and timers, that is, a microcontroller is an IC with a CPU microprocessor; hence a microprocessor arranged as a part of a microcontroller is an IC with core circuitry and use of the JTAG circuitry taught in the Whetsel patent in a microprocessor arranged as a part of a microcontroller is a particular obvious embodiment of the Whetsel patent since a microprocessor arranged as a part of a microcontroller is an IC with core circuitry.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of the Whetsel patent by including use of the JTAG circuitry taught in the Whetsel patent in a microprocessor arranged as a part of a microcontroller. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of the JTAG circuitry taught in the Whetsel patent in a microprocessor arranged as a part of a microcontroller would have provided the opportunity to implement the JTAG circuitry taught in the Whetsel patent in a particular embodiment of an IC with core circuitry for which it was designed.

However Whetsel does not explicitly teach the specific use of a boundary scan test procedure may occur without external access to the JTAG interface.

Hellebrand, in an analogous art, teaches use of a boundary scan test procedure may occur without external access to the JTAG interface (column 2 and Figure 1 of page 195 in Hellebrand teach an embedded processor for carrying out BIST scan testing using a

boundary scan test procedure may occur without external access to the JTAG interface).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Whetsel with the teachings of Hellebrand by including use of a boundary scan test procedure may occur without external access to the JTAG interface. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a boundary scan test procedure may occur without external access to the JTAG interface would have provided the opportunity to split BIST scan testing between software and hardware (column 1 and Figure 1 of page 195 in Hellebrand).

35 U.S.C. 103(a) rejection of claim 3.

Whetsel teaches inputting a stipulated test sequence in the test routine to the pins of the JTAG interface (test routine data provided at TDI 26 in Figure 2 of Whetsel is a stipulated test sequence in the test routine inputted to the pins of the JTAG interface), and reading a sequence of output values at the pins of the JTAG interface corresponding to the stipulated test sequence in the test routine (results of test routine data provided at TDI 26 in Figure 2 of Whetsel is a sequence of output values at the pins of the JTAG interface corresponding to the stipulated test sequence in the test routine).

35 U.S.C. 103(a) rejection of claim 4.

Whetsel teaches the test routine on TDI pin 26 of Figure 2 in Whetsel causes the IC to provide a test result data stream to the JTAG interface to be outputted at TDO pin 27 within the framework of the boundary scan test procedure.

35 U.S.C. 103(a) rejection of claim 5.

Whetsel teaches switching the I/O ports of the IC core circuitry corresponding toTAP1-TAP4 in figure 2 of Whetsel to transmit the test routine for a predefined duration to output ports TDO1-TDO4 and to high (col. 4, lines 25-28 in Whetsel teach high is used to select a TAP along with its output); and measuring levels present at an interface of the microcontroller (JTAG boundary scan circuitry is composed of output scan elements used to measure the level at the output of a circuit).

35 U.S.C. 103(a) rejection of claim 6.

Whetsel teaches switching the I/O ports of the IC core circuitry to input ports to enable reception of values from the pins 20 in Figure 2 of Whetsel of the JTAG interface TAP1-TAP4 generated by the test routine for a predefined duration; and applying defined values to an interface of the IC core circuitry to transmit the stipulated test sequence to the IC core circuitry (TDI input at TDI pin 26 applies defined values to an interface TAP1-TAP4 of the IC core circuitry to transmit the stipulated test sequence to the IC core circuitry).

35 U.S.C. 103(a) rejection of claim 7.

Whetsel teaches reading out the values present at the pins of the JTAG interface and stored in the memory area via the interface of the IC core circuitry (JTAG Boundary Scan Registers are memory for reading out the values present at the pins of the JTAG interface and storing the values in the JTAG Boundary Scan Register memory area via the interface of the IC core circuitry).

35 U.S.C. 103(a) rejection of claim 8.

Whetsel teaches reading out the values present at the pins of the JTAG interface and stored in the memory area via the interface of the IC core circuitry (JTAG Boundary Scan Registers are memory for reading out the values present at the pins of the JTAG interface and stored in the JTAG Boundary Scan Register memory area via the interface of the IC core circuitry).

35 U.S.C. 103(a) rejection of claim 10.

Whetsel teaches at least one microprocessor capable of being activated, within a framework of a boundary scan test procedure as set forth in IEEE standard 1149 using a JTAG interface of the at least one microprocessor (the Abstract and Figure 2 of Whetsel teaches a device for activating IEEE 1149.1 compliant test access ports for an IC comprising multiple IEEE 1149.1 compliant test access ports for testing core circuitry in the IC as shown in Figure 18 of Whetsel; Col. 17, lines 7-36 in Whetsel teach an application and embodiment whereby the IC is a microprocessor; Note: an IEEE 1149.1

compliant tests access port is a JTAG interface, hence Whetsel teaches a method for activating a microprocessor for Boundary Scan testing, within a framework of a boundary scan test procedure as set forth in IEEE standard 1149 using at least one IEEE 1149.1 compliant test access port of the microprocessor, i.e., at least one JTAG interface), wherein: the at least one microprocessor is configured to execute a test routine and includes an arrangement for activating the JTAG interface using the test routine (the Abstract and Figure 2 of Whetsel teaches that TAP linking module 21 is used for activating at least one IC IEEE 1149.1 compliant test access ports, i.e., at least one JTAG interface; col.4, lines 25-28 in Whetsel teach that during testing the TLM is selected as the data register's scan path between the IC's TDI and TDO scan path used for providing the IC with test routine data; col.4, lines 40-42 in Whetsel teach that test routine data provided to the TLM on the TDI input is used to select one of the 4 enable signals EN1-4 for activating at least one of the IC IEEE 1149.1 compliant test access ports corresponding to the enable signal), the arrangement including PAD cells of the microprocessor and connecting leads from the PAD cells to data-in and data-out pins of the JTAG interface (Note: each of the I/O ports, TDI, TDO1-TDO4 of the IC core circuitry are connected to TDI pin 26 and TDO pin 27 hence TDI pin 26 and TDO pin 27 are pins for each of the TAP1-TAP4 JTAG interfaces, that is, I/O ports, TDI, TDO1-TDO4, of the IC core circuitry are connected to TDI pin 26 and TDO pin 27 pins of the JTAG interface; in addition, TDI pin 26 is the data-in pin for each of the TAP1-TAP4 JTAG interfaces, hence when any of the TAP1-TAP4 JTAG interfaces are activated, the TDI data-in pin 26 for the activated TAP1-TAP4 JTAG interfaces is also activated to

provide test routine data to the activated TAP1-TAP4 JTAG interfaces and is activated using the test routine data by providing the test routine data to the TLM), the PAD cells including an input/output port function (Note: activating a TAP1-TAP4 JTAG interface is an input/output port function; Note also IC pins generally have PAD cells for controlling input and output to the IC pin).

However Whetsel does not explicitly teach that the IC taught in the Whetsel patent is a microprocessor arranged as a part of a microcontroller.

Webopedia (http://www.webopedia.com/TERM/m/microcontroller.html) defines a microcontroller as a highly integrated IC chip that contains all the components comprising a controller, typically, including a CPU, RAM, some form of ROM, I/O ports, and timers, that is, a microcontroller is an IC with a CPU microprocessor; hence a microprocessor arranged as a part of a microcontroller is an IC with core circuitry and use of the JTAG circuitry taught in the Whetsel patent in a microprocessor arranged as a part of a microcontroller is a particular obvious embodiment of the Whetsel patent since a microprocessor arranged as a part of a microcontroller is an IC with core circuitry.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of the Whetsel patent by including use of the JTAG circuitry taught in the Whetsel patent in a microprocessor arranged as a part of a microcontroller. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of the JTAG circuitry taught in the Whetsel patent in a

microprocessor arranged as a part of a microcontroller would have provided the opportunity to implement the JTAG circuitry taught in the Whetsel patent in a particular embodiment of an IC with core circuitry for which it was designed.

However Whetsel does not explicitly teach the specific use of a boundary scan test procedure may occur without external access to the JTAG interface.

Hellebrand, in an analogous art, teaches use of a boundary scan test procedure may occur without external access to the JTAG interface (column 2 and Figure 1 of page 195 in Hellebrand teach an embedded processor for carrying out BIST scan testing using a boundary scan test procedure may occur without external access to the JTAG interface).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Whetsel with the teachings of Hellebrand by including use of a boundary scan test procedure may occur without external access to the JTAG interface. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a boundary scan test procedure may occur without external access to the JTAG interface would have provided the opportunity to split BIST scan testing between software and hardware (column 1 and Figure 1 of page 195 in Hellebrand).

35 U.S.C. 103(a) rejection of claim 12.

Whetsel teaches the microcontroller includes an interface to external devices, the

interface enabling output levels present at the interface to be measured and enabling inputs of defined values by an external device (JTAG interface 20 in Figure 2 is an interface to external devices, the interface enabling output levels present at the interface to be measured and enabling inputs of defined values by an external device).

4. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Whetsel; Lee D. (US 6408413 B1) and Hellebrand et al. (Hellebrand, S.; Wunderlich, H.-J.; Hertwig, A.; **Mixed-mode BIST using embedded processors,** Proceedings International Test Conference, 20-25 Oct. 1996 Page(s):195 – 204, hereafter referred to as Hellebrand) in view of Margolis, Donald L. et al. (US 5357432 A, hereafter referred to as Margolis).

35 U.S.C. 103(a) rejection of claim 9.

Whetsel and Hellebrand, substantially teaches the claimed invention described in claims 1 and 3-8 (as rejected above).

However Whetsel and Hellebrand, does not explicitly teach the specific use of the IC core circuitry with microprocessor taught in the Zuraski patent **for a motor vehicle**.

Margolis, in an analogous art, teaches a microcontroller for use in a sensing system for a motor vehicle (col. 4, lines 60-68, Margolis). The Examiner asserts that it would be obvious to use the IC core circuitry with a microprocessor taught in the Whetsel patent since that is one of the uses for which IC core circuitry with a microprocessor is designed for. One of ordinary skill in the art at the time the invention was made would

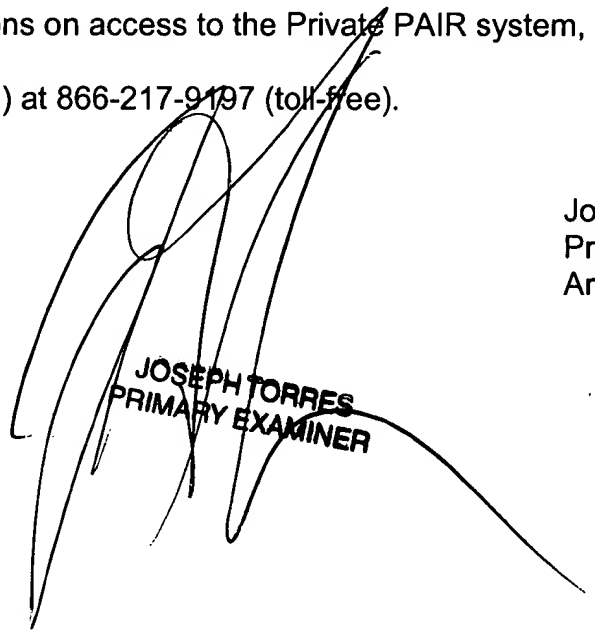
have been highly motivated to use the IC core circuitry with a microprocessor taught in the Whetsel patent in a motor vehicle because the IC core circuitry with a microprocessor taught in the Whetsel patent has the added feature of Built-In Self-Test (BIST) logic which provides the ability to test for circuit integrity (see Abstract, Whetsel). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Whetsel and Hellebrand with the teachings of Margolis by including use of the IC core circuitry with a microprocessor taught in the Whetsel patent in a motor vehicle. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of the IC core circuitry with a microprocessor taught in the Whetsel patent in a motor vehicle would provide the opportunity to test for circuit integrity (see Abstract, Whetsel).

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (571) 272-3829. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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